CLAIMS

What is claimed is:

1. A Schottky diode comprising:

a conductive anode contact;

a semiconductor layer supporting the conductive contact, the conductive anode contact and the semiconductor layer forming a diode junction;

a base layer ring formed around at least a portion of the conductive anode contact; and

a base layer material gap adjacent to the conductive anode contact formed in the base layer ring.

2. The diode of claim 1, further comprising a dielectric layer supported by the base layer ring and abutting the conductive contact.

3. The diode of claim 2, wherein the base layer material gap is a vacuum gap bounded by at least the conductive anode contact and the base layer ring.

4. The diode of claim 3, wherein the base layer material gap is further bounded by the dielectric layer and the semiconductor layer.

5. The diode of claim 2, wherein the base layer material gap is a non-vacuum gap bounded by at least the conductive anode contact and the base layer ring.

6. The diode of claim 5, wherein the base layer material gap is further bounded by the dielectric layer and the semiconductor layer.

7. The diode of claim 2, wherein the conductive anode contact is metallic and the semiconductor layer is Indium Phosphide.

8. The diode of claim 1, wherein the conductive anode contact comprises layers of different metals.

9. The diode of claim 8, wherein the conductive contact comprises a layer of Titanium adjacent to the semiconductor material supporting a layer of Platinum supporting a layer of Gold.

10. The diode of claim 8, wherein the conductive contact comprises a layer of Platinum supporting a layer of Titanium supporting an additional layer of Platinum supporting a layer of Gold.

11. The diode of claim 1, wherein the base layer material gap is sized in accordance with an expected extent of a reverse bias depletion region in the semiconductor layer.

12. A method for fabricating a diode, the method comprising:

creating a semiconductor layer on a substrate;

creating a base layer on the semiconductor layer;

creating a dielectric layer on the base layer;

removing a portion of the dielectric layer to form a via through the dielectric layer to the base layer;

laterally removing a portion of the base layer underneath the dielectric layer and through to the semiconductor layer at the via; and

creating a conductive anode contact in the via supported by the semiconductor layer, the conductive anode contact bounding a base layer gap between the conductive anode contact and the base layer ring.

13. The method of claim 12, wherein laterally removing further comprises laterally removing a portion of the base layer sized in accordance with an expected extent of a reverse bias depletion region in the semiconductor layer.

14. The method of claim 12, wherein creating a conductive anode comprises vacuum depositing a conductive anode.

15. The method of claim 12, wherein creating a conductive anode comprises depositing a layer of Titanium adjacent to the semiconductor material, a layer of Platinum, and a layer of Gold.

16. The method of claim 12, wherein creating a conductive anode comprises depositing a layer of Platinum adjacent to the semiconductor material, a layer of Titanium, a layer of Platinum, and a layer of Gold.

17. The method of claim 12, wherein creating a base layer further comprises creating a base layer using a different material than the dielectric layer.

18. The method of claim 17, wherein creating a base layer further comprises creating an Indium-Gallium-Arsenide base layer.

19. The method of claim 17, wherein laterally removing comprises wet etching a portion of the base layer to remove material underneath the dielectric layer and through to the semiconductor layer at the via.

20. A method for fabricating a diode, the method comprising:

creating a semiconductor layer on a substrate;

creating a base layer on the semiconductor layer;

creating a first dielectric layer on the base layer;

removing a portion of the first dielectric layer to form a via through the dielectric layer to the base layer;

laterally removing a portion of the base layer underneath the dielectric layer and through to the semiconductor layer at the via; and

creating a conductive anode layer in the via supported by the semiconductor layer;

sealing the via using a second dielectric layer;

removing a second portion of the second dielectric layer to expose the conductive anode layer; and

creating a conductive anode connection to the conductive anode layer.

21. The method of claim 20, wherein laterally removing further comprises laterally removing a portion of the base layer sized in accordance with an expected extent of a reverse bias depletion region in the semiconductor layer.

22. The method of claim 20, wherein creating a conductive anode layer comprises depositing a layer of Titanium adjacent to the semiconductor material, and wherein creating a conductive anode connection comprises depositing a layer of Platinum and a layer of Gold on the conductive anode layer.

23. The method of claim 20, wherein creating a conductive anode layer comprises depositing a first layer of Platinum adjacent to the semiconductor material, and wherein creating a conductive anode connection comprises depositing a second layer of Titanium, a layer of Platinum, and a layer of Gold on the conductive anode layer.

24. The method of claim 20, wherein creating a base layer further comprises creating a base layer using a different material than the dielectric layer, and wherein laterally removing comprises wet etching.